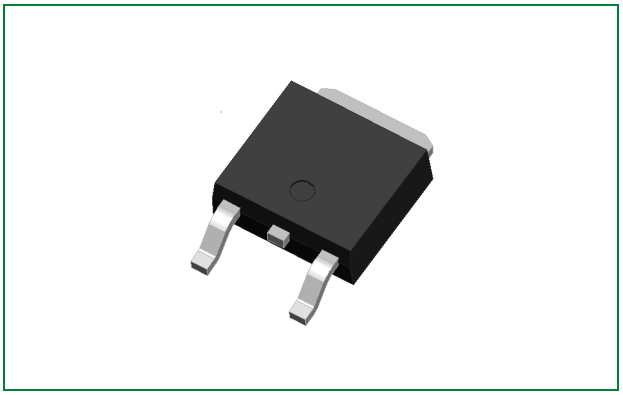
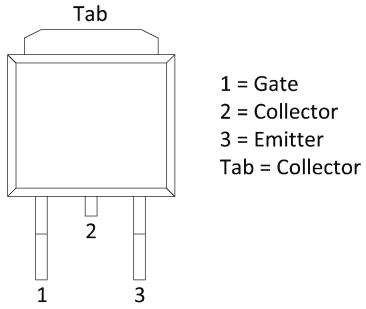
LGD8209TI
410 V, 12 A N-Channel Ignition IGBT



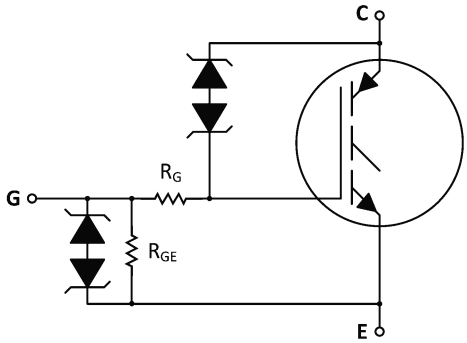
Agency Approvals and Environmental

Environmental Approvals
Pb

Pinout Diagram



Functional Diagram



Product Summary

Characteristic	Value	Unit
V_{CES}	410	V
I_C	12	A

Description

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over-Voltage clamped protection for use in inductive coil drivers applications. Primary uses include motorbike ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

Features

- Ideal for Coil-on-Plug Applications
- DPAK Package Offers Smaller Footprint and Increased Board Space
- Gate-Emitter ESD Protection
- Temperature Compensated Gate-Collector Voltage Clamp Limits Stress Applied to Load
- Low Saturation Voltage
- High Pulsed Current Capability
- These are Pb-Free Devices

1. Maximum Ratings (T_J = 25 °C unless otherwise specified)

Characteristic	Conditions	Symbol	Value	Unit
Collector-Emitter Voltage	-	V_{CES}	445	V_{DC}
Collector-Gate Voltage	-	V_{CER}	445	V_{DC}
Gate-Emitter Voltage	-	V_{GE}	15	V_{DC}
Collector Current – Continuous		I_C	12	A_{DC}
Collector Current – Pulsed	T_C = 25 °C		30	A_{AC}
ESD – Human Body Model	R = 1500 Ω, C = 100 pF	ESD	8.0	kV
ESD – Machine Model	R = 0 Ω, C = 200 pF		800	V
Total Power Dissipation	T_C = 25 °C	P_D	94	W
	Derating for > 25 °C		0.63	W/°C
Operating and Storage Temperature Range	-	T_J, T_{stg}	–55 to +175	°C

2. Unclamped Collector-to-Emitter Avalanche Characteristics

Characteristic	Symbol	Value	Unit
Single Pulse Collector-to-Emitter Avalanche Energy			
V_{CC} = 50 V, V_{GE} = 5.0 V, P_kI_L = 7.4 A, L = 10 mH, Starting T_J = 25 °C	E_{AS}	274	mJ

3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.6	°C/W
Thermal Resistance, Junction to Ambient (DPAK)[1]	$R_{\theta JA}$	105	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Footnote 1: When surface mounted to an FR4 board using the minimum recommended pad size

4. Electrical Characteristics – Off

Characteristic	Symbol	Conditions	Temperature	Value			Unit
				Min	Typ	Max	
Collector-Emitter Clamp Voltage	BV_{CES}	I_C = 2.0 mA	T_J = –40 °C to 150 °C	380	410	435	V_{DC}
		I_C = 10 mA		340	420	445	
Zero Gate Voltage Collector Current	I_{CES}	V_{CE} = 350 V, V_{GE} = 0 V	T_J = 25 °C	-	1.0	25	μA_{DC}
			T_J = 150 °C	-	9.0	50	
			T_J = –40 °C	-	0.5	15	
Reverse Collector-Emitter Leakage Current	I_{ECS}	V_{CE} = –24 V	T_J = 25 °C	-	0.5	1.0	mA
			T_J = 150 °C	-	10	30	
			T_J = –40 °C	-	0.05	0.5	
Reverse Collector-Emitter Clamp Voltage	$BV_{CES(R)}$	I_C = -75 mA	T_J = 25 °C	26	33	38	V_{DC}
			T_J = 150 °C	29	36	41	
			T_J = –40 °C	24	32	36	
Gate-Emitter Clamp Voltage	BV_{GES}	I_G = 5.0 mA	T_J = –40 °C to 150 °C	10	13	16	V_{DC}
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = 10 V	T_J = –40 °C to 150 °C	380	635	1000	μA_{DC}
Gate Resistor	R_G	-	T_J = –40 °C to 150 °C	-	70	-	Ω
Gate-Emitter Resistor	R_{GE}	-	T_J = –40 °C to 150 °C	10	16	26	kΩ

5. Electrical Characteristics – On

Characteristic	Symbol	Conditions	Temperature	Value			Unit
				Min	Typ	Max	
Gate Threshold Voltage	$V_{GE(th)}$	I_C = 1.0 mA, V_{GE} = V_{CE}	T_J = 25 °C	1.0	1.42	2.0	V_{DC}
			T_J = 150 °C	0.7	0.95	1.5	
			T_J = –40 °C	1.1	1.62	2.2	
Threshold Temperature Coefficient (Negative)	-	-	-	-	3.5	-	mV/°C
Collector-Emitter On-Voltage[2]	$V_{CE(on)}$	I_C = 6.0 A, V_{GE} = 4.0 V	T_J = 25 °C	0.8	1.45	2.0	V_{DC}
			T_J = 150 °C	0.85	1.44	1.85	
			T_J = –40 °C	1.0	1.5	1.95	
		I_C = 10 A, V_{GE} = 4.5 V	T_J = 25 °C	1.1	1.79	2.3	
			T_J = 150 °C	1.2	1.9	2.2	
			T_J = –40 °C	1.3	1.77	2.2	
Forward Transconductance	gfs	V_{CE} = 5.0 V, I_C = 6.0 A	T_J = -40 °C to 150 °C	5.0	14	30	Mhos

Footnote 2: Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%

6. Figure Data

Figure 1. Output Characteristics (T_J = 25 °C)

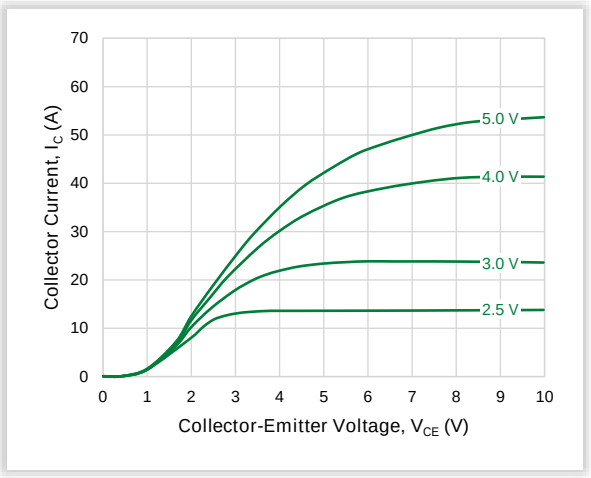


Figure 2. Output Characteristics (T_J = -40 °C)

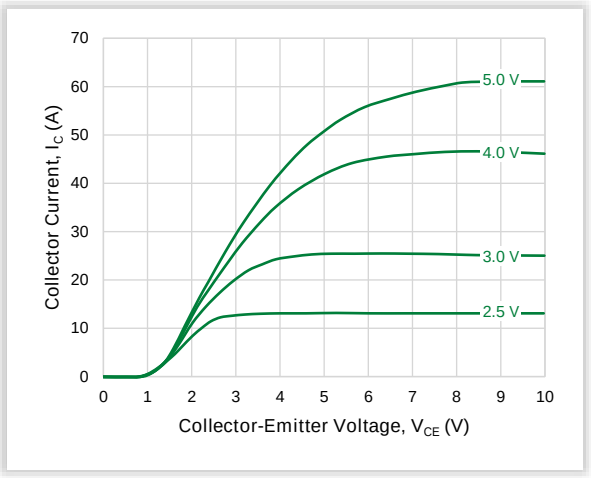


Figure 3. Output Characteristics (T_J = 150 °C)

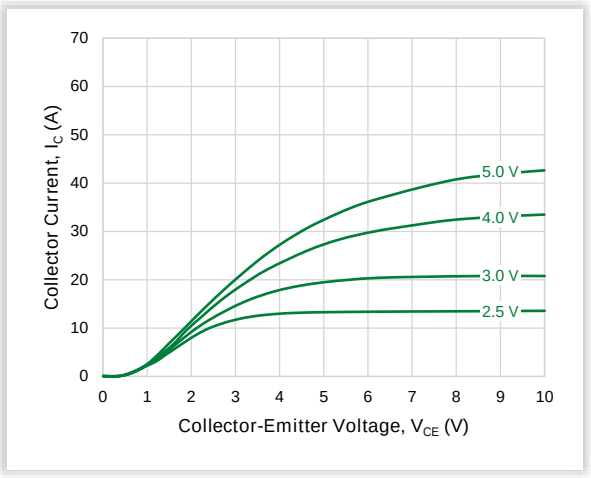


Figure 4. Transfer Characteristics

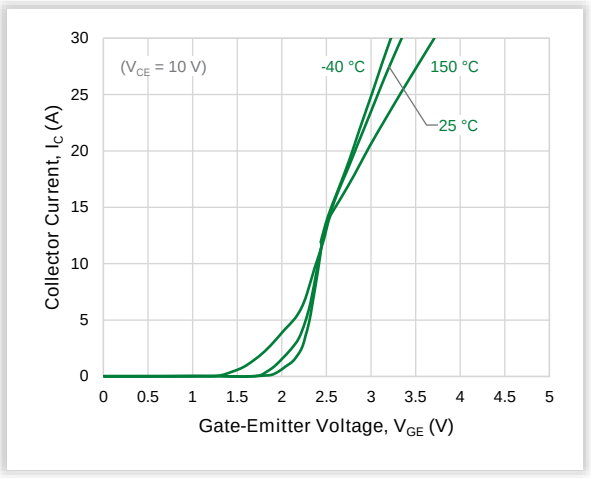


Figure 5. Collector-to-Emitter Saturation Voltage vs. Junction Temperature

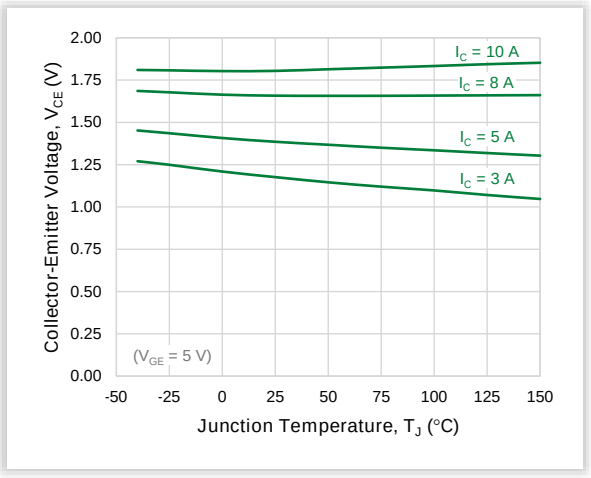


Figure 6. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

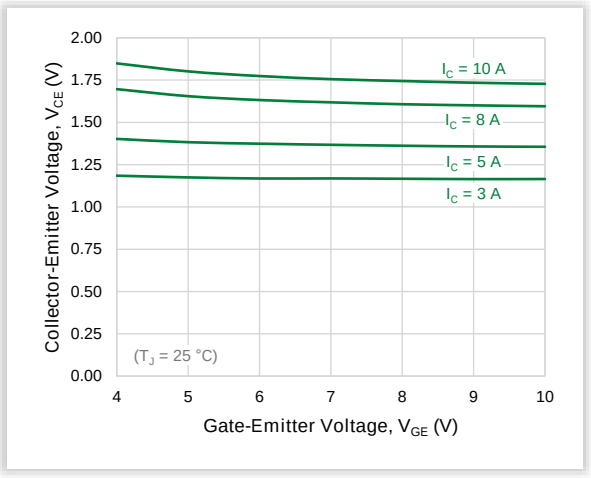


Figure 7. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

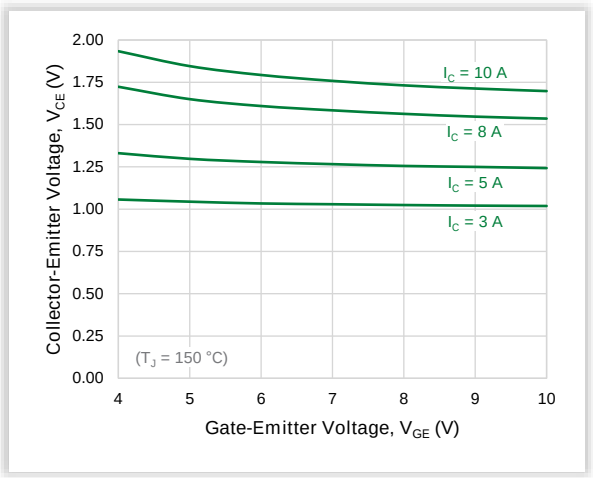
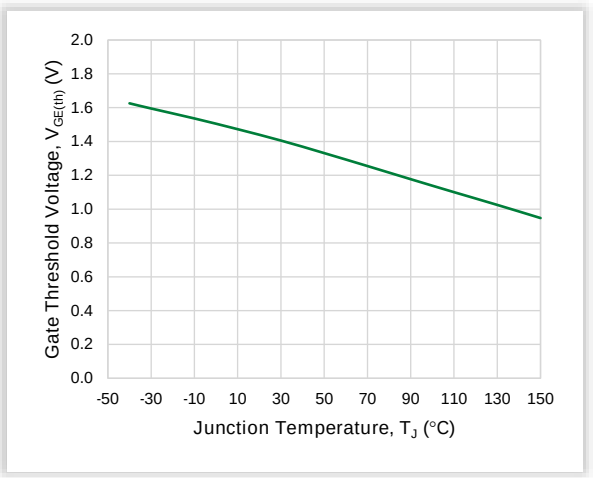
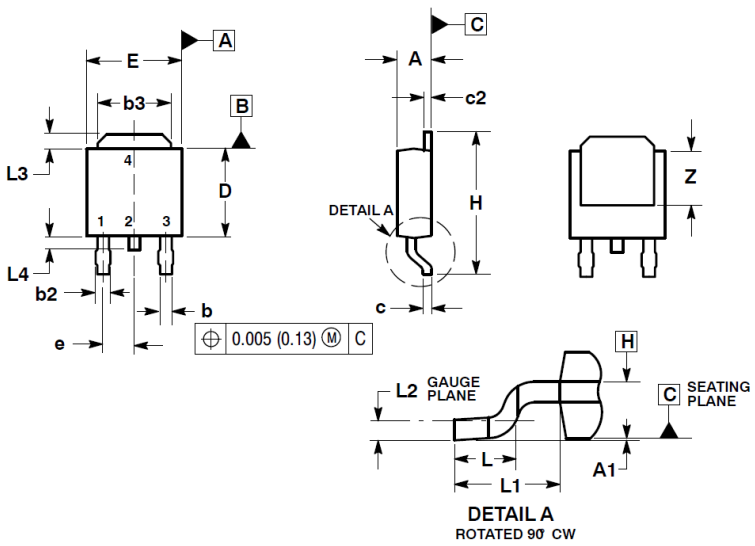


Figure 8. Gate Threshold Voltage vs. Junction Temperature

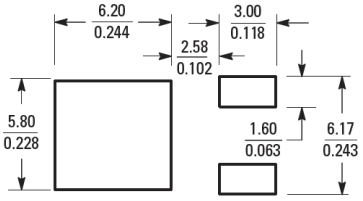


7. Package Dimensions



Symbol	Millimeters		
	Min	Nom	Max
A	2.18	-	2.38
A1	0.00	-	0.13
b	0.63	-	0.89
b2	0.76	-	1.14
b3	4.57	-	5.46
c	0.46	-	0.61
c2	0.46	-	0.61
D	5.97	-	6.22
E	6.35	-	6.73
e	2.29 BSC		
H	9.40	-	10.41
L	1.40	-	1.78
L1	2.74 REF		
L2	0.51 BSC		
L3	0.89	-	1.27
L4	-	-	1.01
Z	3.93	-	-

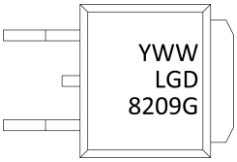
Recommended Solder Pad Layout:



Notes:

1. Dimensioning and tolerancing per ASME Y14.5M, 1994.
2. Controlling dimension: Inches.
3. Thermal pad contour optional within dimensions b3, L3, and Z.
4. Dimensions D and E do note include mild flash, protrusions, or burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 inches per side.
5. Dimensions D and E are determined at the outermost extremes of the plastic body.
6. Datums A and B are determined at datum plane H.

8. Part Numbering and Marking



LGD8209G	= Device Code
Y	= Year
WW	= Work Week

9. Packing Options

Part Number	Package	Packing Mode	M.O.Q.
LGD8209TI	DPAK (Pb-Free)	Tape & Reel	2500

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